**ELEC6200 Computer Architecture and Design** N.S.V.Ravi Tej Uppu

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CPU Design Project

Report

The main objective of the project was to design a 16-bit RISC processor using MODELSIM as a design tool and to implement it on Altera kit using QuartusII software. The processor designed has a Multicycle datapath and a Finite state machine as its control unit, the ISA (instruction set architecture) for this processor has 16-core instructions (7 R-type instructions, 7 I-type instructions and 2 jump instructions) and the basic instruction format is chosen accordingly. From this project I came to know that instructions are categorized based on their instruction format (though my immediate instructions are I-type they are executed as an R-type instruction with different control signals in R-type states of the FSM) besides I also got good intuition in programing using VHDL language, also I learned how to debug a code which seems to be working initially. Finally, this project helped me in getting the insight of what we learned in the class.

If I were to design a Processor again I would definitely choose Pipelining as my datapath and a Microcomputer as its control unit (using microprogramming and micro instructions) also I would try to make effective use of the registers defined and check for the functionality of the processor for implementing ‘procedures’ and ‘functions’ with a good hazard detection and forwarding unit.

My advise to the students who are going to work on a similar project is to start the project as early as possible by optimizing the datapath chosen according to the instruction set architecture (ISA). From my experience I would say that if a student has complete overview of their respective datapath and the functionality of their control unit the only problem would be with the coding part in modelsim which can be dealt deftly by knowing fundamentals of VHDL and being in regular contact with the TA by updating status of the project.

In conclusion, I have thoroughly enjoyed on each stage of the CPU design project and gained invaluable experience in the design and functioning of a practical processor. I fell that the knowledge I gained in the course of doing this project as a great asset for my future endeavors.